Amendments to the Claims:

Please cancel claims 4, 8, 10 and 12.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A differential charge pump comprising:

a first driver for receiving a first input signal and generating a first output signal;

a second driver for receiving a second input signal and generating a second output signal;

a third driver for receiving an inverted signal of the second input signal and generating a third output signal having the same voltage level as the first output signal;

a fourth driver for receiving an inverted signal of the first input signal and generating a fourth output signal having the same voltage level as the second output signal;

a first transistor having a gate connected to a first bias voltage, a source to which the first output signal is applied, and a drain connected to an output signal of a first differential charge pump;

a second transistor having a gate connected to the first bias voltage, a source to which the second output signal is applied, and a drain connected to an output signal of a second differential charge pump;

a third transistor having a gate connected to [[the]] a second bias voltage, a source to which the third output signal is applied, and a drain connected to an output signal of the first differential charge pump: [[and]]

a fourth transistor having a gate connected to [[a]] the second bias voltage, a source to which the fourth output signal is applied, and a drain connected to the output signal of the second differential charge pump;

a reference voltage generating circuit for generating a reference voltage;

a reference current generating circuit for generating a reference current and having its output connected to the second bias voltage;

a common mode feedback circuit for receiving the output of the reference voltage, the output signal of the first differential charge pump and the output signal of the second differential charge pump as inputs and generating the first bias voltage; and

a fifth transistor having a drain and a gate connected to the second bias voltage, and a source connected to the ground voltage.

2. (Original) The differential charge pump according to claim 1, wherein the first input signal is a down signal, and the second input signal is an up signal, and the first to the fourth drivers are buffers.

3. (Original) The differential charge pump according to claim 1, wherein the first input signal is an inverted down signal, and the second input signal is an inverted up signal, and the first to the fourth drivers are inverters.

4. (Canceled)

5. (Currently Amended) A phase locked loop having a phase detection means for detecting a phase difference between a reference clock signal and a desired clock signal and generating a first input signal, a second input signal, an inverted signal of the first input signal and an inverted signal of the second input signal;

a differential charge pump for receiving the first input signal, the second input signal, the inverted signal of the first input signal and the inverted signal of the second input signal as input signals and generating an output signal of a first differential charge pump and an output signal of a second differential charge pump;

a loop filter for charging and discharging in response to the output signal of the first differential charge pump and the output signal of the second differential charge pump; and

a voltage controlled oscillator for receiving the output signal of the first differential charge pump and the output signal of the second differential charge pump as input signals and

controlling the phase of the desired clock signal, wherein the differential charge pump comprises:

a first driver for receiving a first input signal and generating a first output signal;

a second driver for receiving a second input signal and generating a second output signal;

a third driver for receiving an inverted signal of the second input signal and generating a third output signal having the same voltage level with the first output signal;

a fourth driver for receiving an inverted signal of the first input signal and generating a fourth output signal having the same voltage level with the second output signal;

a first transistor having a gate connected to a first bias voltage, a source to which the first output signal is applied, and a drain connected to an output signal of a first differential charge pump;

a second transistor having a gate connected to the first bias voltage, a source to which the second output signal is applied, and a drain connected to an output signal of a second differential charge pump;

a third transistor having a gate connected to [[the]] a second bias voltage, a source to which the third output signal is applied, and a drain connected to an output signal of the first differential charge pump: [[and]]

a fourth transistor having a gate connected to [[a]] the second bias voltage, a source to which the fourth output signal is applied, and a drain connected to the output signal of the second differential charge pump;

a reference voltage generating circuit for generating a reference voltage;

a reference current generating circuit for generating a reference current and having its output connected to the second bias voltage;

a common mode feedback circuit for receiving the output of the reference voltage, the output signal of the first differential charge pump and the output signal of the second differential charge pump as inputs and generating the first bias voltage; and

a fifth transistor having a drain and a gate connected to the second bias voltage, and a source connected to the ground voltage.

6. (Original) The phase locked loop according to claim 5, wherein the first input signal is a down signal, and the second input signal is an up signal, and

the first to the fourth drivers are buffers.

7. (Original) The phase locked loop according to claim 5, wherein the first input signal is an inverted down signal, and the second input signal is an inverted up signal, and

the first to the fourth drivers are inverters.

8. (Canceled)

9. (Currently Amended) A method for pumping a differential charge pump, comprising:

receiving a first input signal, a second input signal, an

inverted signal of the first input signal and an inverted signal of the second input signal as input signals and generating a first output signal, a second output signal, a third output signal having the same level with the first output signal, and a fourth output signal having the same level with the second output signal; and

controlling a voltage level of the first output signal by a first bias voltage, controlling a voltage level of the third output signal by a second bias voltage and then generating an output signal of a first differential charge pump, controlling a voltage level of the second output signal by the first bias voltage, controlling a voltage level of the fourth output signal by the second bias voltage and then generating an output signal of a second differential charge pump, receiving a reference voltage and the output signals of the first and second differential charge pumps as input signals and generating the first bias voltage, and generating the second bias voltage using the reference current.

10. (Canceled)

11. (Currently Amended) A method for phase locked looping, comprising:

detecting a phase detect a phase difference between a reference clock signal and a desired clock signal and generating a first input signal, a second input signal, an inverted signal of the first input signal, and an inverted signal of the second input signal;

charge pumping to receive a first input signal, a second input signal, an inverted signal of the first input signal, and an inverted signal of the second input signal as input signals and then generating a first output signal, a second output signal, a third output signal having the same level as the first output signal, and a fourth output signal having the same level as the second output signal, and controlling a voltage level of the first output signal by a first bias voltage, controlling a voltage level of the third output signal by a second bias voltage and then generating an output signal of a first differential charge pump, and controlling a voltage level of the second output signal by the first bias voltage, controlling a voltage level of the fourth output signal by the second bias voltage and then generating an output signal of a second differential charge pump, receiving a reference voltage and the output signals of the first and second differential charge pumps as input signals and then generating the first bias voltage, and controlling the second bias voltage using the reference current;

charging and discharging in response to the output signals of the first differential charge pump and the second differential charge pump; and

controlling a phase of the desired clock signal in response to the output signals of the first differential charge pump and the second differential charge pump.

12. (Canceled)